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PSpice Implementation and Simulation of a New Electro-Thermal Modeling for Estimating the Junction Temperature of Low Voltage Power MOSFET

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The estimation of the junction temperature (T_j) is very important factor for improving the reliability and efficiency of the power electronic converters. A new electro-thermal (ET) model of low voltage power MOSFET is described in this paper. The electro-thermal model allows fast estimation of the junction temperature, based on the transient thermal impedances (Z_{th}) using the (R_C) Foster thermal network model and total power losses. The parameters of the (R_C) Foster thermal network model are extracted from the data provided by the manufacturer's datasheet using particle swarm optimization (PSO) method. Moreover, a dc/dc Buck converter is also analyzed by simulation to evaluate the electro-thermal model. The simulation results indicate a good agreement between the proposed model and manufacturer's data. Finally, the electro-thermal (ET) model simulation using this (R_C) Foster thermal network model shows a reasonable accuracy for estimating the junction temperature in a *Dc*/*Dc* buck converter.

Keywords: Electro-thermal model, MOSFET, Junction temperature, Reliability, Particle swarm optimization, PSpice, Buck converter.

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1. INTRODUCTION

The junction temperature (T_j) is one of the most important parameters that influence the performance and behavior of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET).The accurate estimation of the junction temperature (T_j) is thus a key factor. Therefore, a fast and precise transient thermal model based on the junction temperature dependence of the power loss is critical for proper thermal management of power devices. In the technical literature, the methods used to estimate the junction temperature (T_j) of power semiconductors devices are: The first approach is based on numerical methods. It is mainly based on the finite elements method (FEM) that uses a detailed model of the device, and at the same time, it takes into consideration the material proprieties and layers [1, 2]. Providing the exact solution is the success key advantage of this method, nevertheless, it is characterized by its low computation speed in case where different system components with carious time scales are present. This results in a difficult evaluation of the junction temperature evolution in real duty cycle or operating condition. The second approach is based on analytical methods, which is achieved by solving analytical 1D or 2D heat condition diffusion equation. In this method, the estimation of the heat spreading effect might be obtained inaccurately, involving a typical heat spreading angle of 45° [3, 4].The third approach, the most commonly used one, is the equivalent thermal network where circuit simulators are used to estimate the instantaneous junction temperature [5]. As a result of representing the process by a heat transfer coefficient value, this method might not provide a good estimation of the heat convection from the cold plat to the coolant. In this paper an improved electro-thermal (ET) model has been proposed for an accurate junction temperature (T_j) estimation in low voltage power MOSFET model. Particle swarm optimization (PSO) method is used to extract the parameters needed for the construction of (R_C) Foster thermal network model. The coupling of the Foster (R_C) thermal network model and total power loss model is implemented in PSpice circuit simulator. Further, dynamic study of the junction temperature (T_j) and the junction temperature fluctuation (ΔT_j) is also performed by considering the influence of the fundamental frequency. Finally, to better illustrate the capability and attractiveness of the electro-thermal model in estimating the junction temperature (T_j), a *Dc*/*Dc* buck converter is used as a case study.

2. ELECTRO-THERMAL SIMULATION

The diagram of the electro-thermal (ET) simulation model of power MOSFET model is shown in Fig. 1. The total losses model (P_{loss}) of the MOSFET model are composed of the conduction losses (P_{co}) and switching losses (P_{sw}).The total losses model is interfaced with the thermal model as shown in Fig. 1.The electrical loading of converter (current and voltage profiles, switching frequency (f_{sw}) etc.) is first translated into power loss by the device total loss model. This power loss serves as an input of the transient thermal impedance model ($Z_{th\text{-}jc}$), which calculates the junction temperature (T_j), which is then fed back to the total loss model so that the junction temperature dependency of power losses.

2.1. Electrical MOSFET Simulation

The power MOSFET model has been electrically modelled with a PSpice Level 3 model, using datasheet extracted parameters of the [6]. The proposed model is validated with manufacturer's datasheet for the static

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characteristics. Fig. 2 illustrates the simulated and the datasheet by the manufacturer from transfer characteristics at different temperatures (– 55 °C, 25 °C and 125 °C). From the figure, we can see that these comparisons demonstrate good agreement. Moreover, the validity of the model from *I-V* characteristics is verified for different gate voltages at the same temperature. It can be observed from Fig. 3 that the model shows a good agreement at different gate drive voltages.

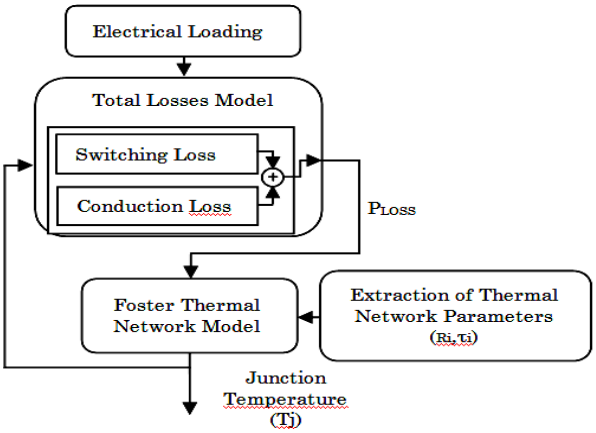


Fig. 1 – The diagram of the electro-thermal (ET) simulation

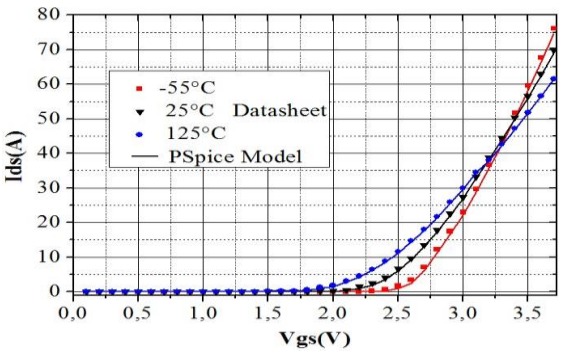


Fig. 2 – Transfer characteristics comparison between the simulation results and datasheet at different temperatures [7]

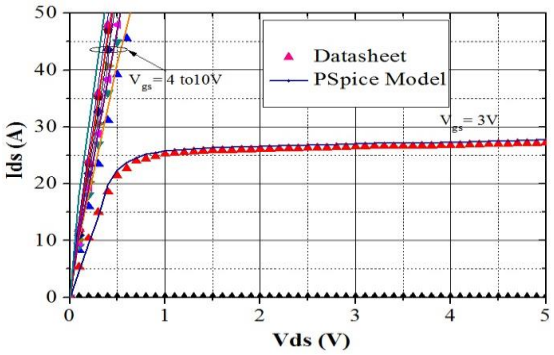


Fig. 3 – *I-V* output characteristics comparison between the simulation results and datasheet for various *Vgs* values at *T* 25 °C [7]

2.2. Thermal Model and Extraction Parameters

The transient thermal behavior of an Metal Oxide Semiconductor Field Effect Transistor (MOSFET) model is characterized by a transient thermal impedance $Z_{th\text{-}jc}(t)$ between the junction and case temperature, can be written as:

$$Z_{th-jc}(t) = \frac{T_j(t) - T_c(t)}{P_d} \quad (1)$$

where $T_j(t)$ is the junction temperature, $T_c(t)$ the case temperature and P_d is the average dissipated power. In order to describe the thermal transient impedance with the required precision, there are two common types of (R_C) network models namely, the Foster and Cauer models [8, 9]. These models provide excellent accuracy over a wide dynamic range, without simulation times or model complexity. A Foster network is constructed using thermal resistance and thermal capacitance parameters from the device datasheet and the parameters do not have physical meanings. In thermal modeling, the Foster R_C network is preferred even though it is purely mathematical. The Foster R_C network can only predict the junction temperature instead of the temperature distribution. In order to improve the Foster thermal networks based models, algorithms are developed for the conversion of Foster networks to an equivalent Cauer type thermal network with the same pair number of R_C lumps [10-12]. The Cauer network relates better to the real physical thermal system because each node represents a real temperature and can be used to describe the temperature distribution inside the packaging [13]. When using the Foster network, the transient thermal impedance curve can be fitted into a series consisting of a finite number of exponential terms as given in (2).

$$Z_{th-jc}(t) = \sum_{i=1}^{n} R_i \left(1 - \exp\left(-\frac{t}{\tau_i}\right)\right) \quad (2)$$

with:

$$\tau_i = R_i C_i \quad (3)$$

The transfer function of (RC) thermal network is obtained by applying the Laplace transform:

$$Z_{th-jc}(s) = \sum_{i=1}^{n} \frac{R_i/\tau_i}{s + 1/\tau_i} \quad (4)$$

In order to extract another (RC) network parameters of the Cauer model, it is necessary to change Eq. (4) as follows (by the following expression) [14, 15]:

$$Z_{th-jc}(s) = \cfrac{1}{sC_{th1} + \cfrac{1}{R_{th1} + \cfrac{1}{sC_{th2} + \ldots \cfrac{1}{R_{th4}}}}} \quad (5)$$

A Cauer thermal network model is based on object's properties and geometry. As with the electrical parameters, the thermal resistance and thermal capacitance are related to the pressure specific heat capacity and thermal conductivity respectively. Thermal resistance R_i and Thermal capacitance C_i are given by:

$$R_i = \frac{d}{\kappa A} \quad (6)$$

$$C_i = CdA\rho \quad (7)$$

where d is the material thickness, A is the cross-sectional area, k is the thermal conductivity, ρ is the density, and c is the pressure specific heat capacity. In the present work, the 4rd order thermal equivalent resistance-capacitance (R_C) Foster model pair parameters are extracted by fitting the step response equation given in (2) to the Zth curves. The (PSO) curve fitting algorithm is used for this purpose. The R_i and τ_i parameters are determined (2) using particle swarm optimization (PSO) method with set population size as 10; inertia weight as between 0.5 and 1; and acceleration factors (c1 and c2): 2 to 2.05 with a maximum iteration set to 1000. In order to estimate the thermal impedance curve provided in the device datasheet according to Fig. 4. It is worth noticing that four parameters are sufficiently enough for a good estimation of the Foster Network. The parameters of the Foster equivalent circuits are extracted. They are listed in Table 1. An excellent correlation can be observed between the RC estimated model and the datasheet. The curve clearly shows that the error between the proposed method and the manufacturer's data does not exceed 1 % which means that the model is accurate.

The extracted parameters of the Foster model and the transformed parameters of the Cauer model are listed in Table 1.

Table 1 – RC parameters of the Foster and equivalent Cauer network model

Foster Model		
N°	$R_i(°C/W)$	$\tau_i(s)$
1	235.2314 10^{-6}	76.3912 10^{-6}
2	812.3754 10^{-3}	1.7798 10^{-3}
3	1.2408	17.5243 10^{-3}
4	1.1465	6.8955 10^{-3}
Cauer Model		
N°	$R_i(°C/W)$	$C_i(J/°C)$
1	154.2246 10^{-3}	375.7561 10^{-6}
2	782.2635 10^{-3}	587.3216 10^{-6}
3	1.1896	5.3214 10^{-3}
4	1.0738	934.2516 10^{-6}

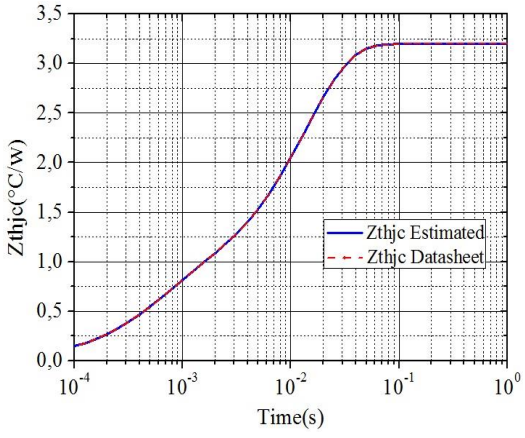


Fig. 4 – Comparison between the transient thermal impedances estimated from PSO method and datasheet model

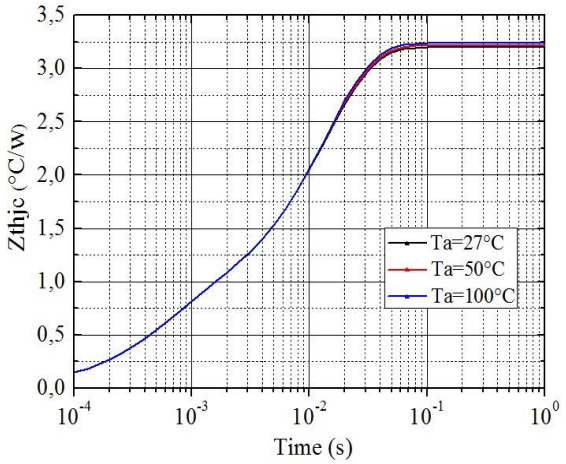


Fig. 5 – Transient thermal impedance under different ambient temperatures

As shown in Fig. 5, for the times less than 0.01s, the differences between the curves is negligible but at higher time instants, the thermal impedances between junction and case Z_{thjc} will be changed relatively and the difference in steady-state conditions is about 2 % between the highest and the lowest thermal impedances. The main reason originates from the dependency of materials thermal conductivity to temperature.

3. (ET) SIMULATION OF A *Dc/Dc* BUCK CONVERTER

To provide a realistic power loss waveform for junction temperature evaluation, a *Dc/Dc* buck converter is constructed in the PSpice software environment, using the electro-thermal model, as shown in Fig. 6. The buck converter circuit, used during the simulation, has been designed to operate at the Switching frequency of 10 kHz with 9 V input voltage, duty ratio $D = 50$ %, the inductance $L = 50$ μH, the output capacitance $C = 50$ μF, and the electrical resistance $R = 4$ Ohm. The power loss profile and the corresponding junction temperature variations during the first 500 μs of simulation time are shown in Fig. 7 and 8.

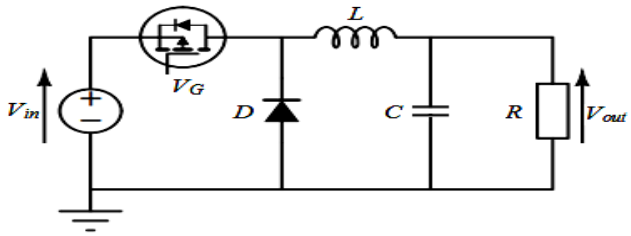


Fig. 6 – Coupled electro-thermal simulation for a *Dc/Dc* buck converter

The dynamic behavior of the junction temperature (T_j) and the corresponding power loss profile based on the proposed electro-thermal model are shown in Fig. 7 and 8. It can be observed that the junction temperature is proportionate to the power loss oscillates at the fundamental frequency, the maximum junction temperature $T_{jmax} = 150$ °C and the junction temperature fluctuates ΔT_j from 143 °C to 150 °C. The abrupt rise of the junction temperature (T_j) at the very beginning and the

junction temperature fluctuations (ΔT_j) during the whole simulation are mainly caused by the small thermal time constant of the MOSFET.

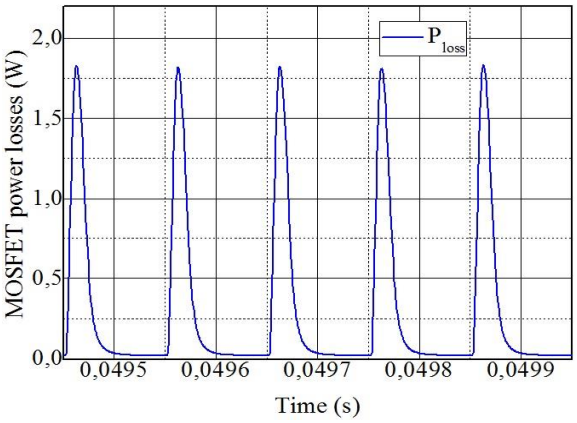


Fig. 7 – The power dissipated in the MOSFET

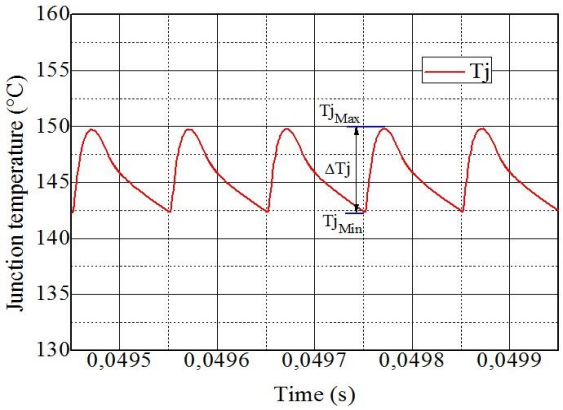
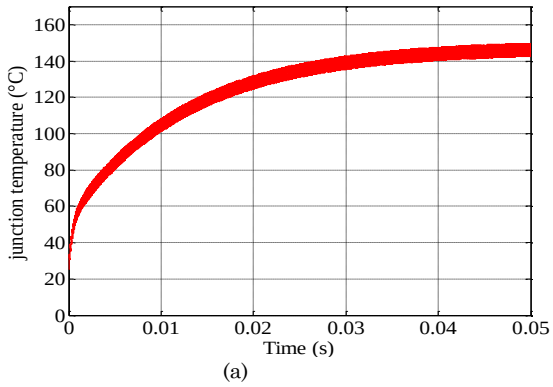


Fig. 8 – The MOSFET junction temperature estimates



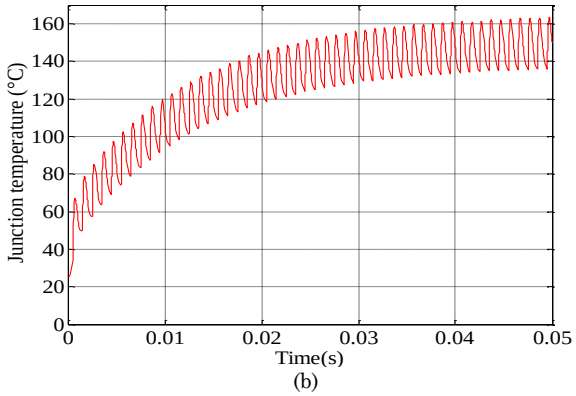


Fig. 9 – Junction temperature waveforms for $f_0 = 50$ Hz (a) and $f_0 = 5$ Hz (b)

In Fig. 9, is shown the comparison of the junction temperature (T_j) waveforms of the MOSFET for different fundamental frequencies (f_0) (50 Hz, 5 Hz). It can be seen that with the decrease of the fundamental frequency, the amplitude of the temperature fluctuation becomes larger.

4. CONCLUSION

This paper proposed a junction temperature (T_j) estimation method for low voltage power MOSFET model in *Dc*/*Dc* buck converter through coupling the transient thermal impedance (Z_{th}) and power loss model. The electro-thermal (ET) model procedure is discussed and the comparisons between simulations results and those provided by the manufacturer's datasheet for the static, dynamic and thermal characteristics behaviors to validate the proposed model are presented. Particle swarm optimization (PSO) method has been used to estimate the parameters for the construction of (R_C) Foster thermal network model. To better illustrate the capability and attractiveness of the (ET) model in estimating the (T_j), the proposed (ET) model is applied to a *Dc*/*Dc* buck converter. Finally, form the simulation results it can be concluded that this model is capable to accurately estimate the (T_j) and ameliorate the system design in order to lowering the maximum (T_j) and to rise the reliability of the system.

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